What I claim is:

1. A semiconductor chip, comprising:

a substrate having a main surface, the main surface including a flame-shaped first area, which is along sides of the main surface, and a second area encompassed by the first area;

a pad formed in the first area;

a bump electrode formed on the pad; and

at least one supporting member formed on the second area.

2. A semiconductor chip as claimed in claim 1, wherein the at least one supporting member comprises a plurality of supporting members.

3. A semiconductor chip as claimed in claim 1, wherein the supporting member is formed of resin material.

4. A semiconductor chip as claimed in claim 1, wherein the supporting member is formed in a center of the second area.

5. A semiconductor chip as claimed in claim 3, wherein the supporting member is formed in a center of the second area.

6. A semiconductor chip as claimed in claim 1, wherein the supporting

member and the bump electrode are formed of the same material.

7. A semiconductor chip as claimed in claim 6, wherein the support member has a first thickness, the pad has a second thickness, the bump electrode has a third thickness, and the first thickness is substantially equal to the sum of the second and third thicknesses.

8. A semiconductor chip as claimed in claim 6, wherein the support member has a first thickness, the pad has a second thickness, the bump electrode has a third thickness, and the first thickness is less than the sum of the second and third thicknesses.

9. A semiconductor chip as claimed in claim 1, further comprising a connector resin formed on the supporting member.

10. A semiconductor chip as claimed in claim 6, further comprising:

a first barrier metal formed under the bump electrode; and

a second barrier metal formed under the supporting member, the first and second barrier metals being formed of the same material, and the first and second barrier metals having the same thickness.

11. A semiconductor package, comprising:

a main substrate having a main surface, the main surface including a flame-shaped first area, which is along sides of the main surface, and a second area encompassed by the first area;

a pad formed in the first area;

a bump electrode formed on the pad;

at least one supporting member formed on the second area;

a tape substrate, which has a main surface and a back surface opposite to the main surface, having a land electrode on the main surface thereof, the land electrode is connected to the bump electrode; and

resin material introduced into a gap, which is formed between the main substrate and the tape substrate.

12. A semiconductor package as claimed in claim 11, wherein the supporting member has a tip that reaches the main surface of the tape substrate.

13. A semiconductor package as claimed in claim 11, wherein the tape substrate further comprises at least one external land electrode formed on the back surface, and a solder ball formed on the external land electrode.

14. A semiconductor package as claimed in claim 13, wherein the external land electrode is arranged under the supporting member.

15. A semiconductor package as claimed in claim 13, wherein:

the at least one supporting member comprises a plurality of supporting members,

the at least one external land electrode and the solder ball thereon comprise a plurality of external land electrodes and solder balls,

the number of supporting members is the same or less than the number of external land electrodes, and

each supporting member is located above one of the external land electrodes.

16. A tape substrate, comprising:

a tape having a main surface, the main surface including a flame-shaped first area, and a second area encompassed by the first area;

a land electrode formed in the first area;

an I/O electrode formed in the first area;

a wiring pattern formed in the first area, the wiring pattern connecting the land electrode to the I/O electrode;

a resist pattern formed on the wiring pattern; and

at least one supporting member formed in the second area.

17. A tape substrate as claimed in claim 16, wherein the supporting member is formed in a center of the second area.

18. A tape substrate as claimed in claim 16, wherein the at least one supporting member comprises a plurality of supporting members.

19. A tape substrate as claimed in claim 17, wherein the support member has a first thickness, the wiring pattern has a second thickness, the resist pattern has a third thickness, and the first thickness is substantially the same as the sum of the second and third thicknesses.

20. A tape substrate as claimed in claim 16, wherein the supporting member and the resist pattern are formed of the same material.

21. A tape substrate as claimed in claim 16, wherein:

the supporting member comprises a first supporting member and a second supporting member formed on the first supporting member,

the first supporting member and the wiring pattern have the same thickness and are formed of the same material, and

the second supporting member and the resist pattern have the same thickness and are formed of the same material.

22. A method of forming a semiconductor chip, comprising:

providing a substrate having a main surface, the main surface including a

flame- shaped first area, which is along sides of the main surface, and a second area encompassed by the first area;

forming a pad in the first area;

forming a bump electrode on the pad; and

forming at least one supporting member on the second area.

23. A method of forming a semiconductor chip as claimed in claim 22, wherein forming the support member includes forming the supporting member of resin material.

24. A method of forming a semiconductor chip as claimed in claim 22, wherein forming the supporting member and the bump electrode includes forming the supporting member and the bump electrode of the same material.

25. A method of forming a semiconductor chip as claimed in claim 24, wherein forming the pad includes forming the pad to have a second thickness, forming the bump electrode includes forming the bump electrode to have a third thickness and forming the support member includes forming the support member to have a first thickness, which is substantially equals to the sum of the second and third thicknesses.

26. A method of forming a semiconductor chip as claimed in claim 24,

wherein forming the pad includes forming the pad to have a second thickness, forming the bump electrode includes forming the bump electrode to have a third thickness and forming the support member includes forming the support member to have a first thickness, which is less than the sum of the second and third thicknesses.

27. A method of forming a semiconductor chip as claimed in claim 24, further comprising, forming a resin connector on the support member.

28. A method of forming a semiconductor package, comprising:

providing a substrate having a main surface, the main surface including a flame- shaped first area, which is along sides of the main surface, and a second area encompassed by the first area;

forming a pad in the first area;

forming a bump electrode on the pad;

forming at least one supporting member on the second area;

providing a tape substrate having a land electrode;

connecting the bump electrode to the land electrode; and

connecting the supporting member to the tape substrate.

29. A method of forming a semiconductor package as claimed in claim 28, wherein connecting the supporting member to the tape substrate includes connecting the supporting member to the tape substrate by a connector resin.

30. A method of forming a semiconductor package as claimed in claim 28, wherein the tape substrate further includes a dummy land electrode, and connecting the supporting member to the tape substrate includes connecting the supporting member to the tape substrate by connecting the tape substrate to the dummy land electrode.

31. A method of forming a semiconductor package, comprising:

providing a semiconductor chip including a main substrate having a main surface, the main surface including a flame-shaped first area, which is along sides of the main surface, and a second area encompassed by the first area, a pad formed in the first area, a bump electrode formed on the pad, and at least one supporting member formed on the second area;

preparing an assemble apparatus having a recess at its center;

providing a tape substrate having a land electrode;

placing the tape substrate on the assemble apparatus wherein an area on the tape substrate, which is encompassed by the land electrode, is disposed on the recess of the assemble apparatus; and

mounting the semiconductor chip on the tape substrate, and connecting the bump electrode to the land electrode.